# MICROPROCESSORS AND MICROSYSTEMS

## Index to Volume 19 (1995)


No 1 pp 1–64
No 2 pp 65–112
No 3 pp 113–176
No 4 pp 177–240
No 5 pp 241–308
No 6 pp 309–380
No 7 pp 381–444
No 8 pp 445–500
No 9 pp 501–556
No 10 pp 557–628


### Article index


**Number 1**

A high-performance analogue input/output system for transputer applications
*J. R. Elphick, T. Clarke and S. T. Lawes* 3
Genetic algorithms for generating minimum path configurations
*P. K. Sharpe, A. G. Chalmers and A. Greenwood* 9
Design and testing of a PI controller ASIC
*I. A. Grout, S. E. Burge and A. P. Dorey* 15
Evaluation of the Data Interaction Architecture Demonstrator by means of a multiple mobile robot workspace simulation
*F. Xia, S. A. Velastin and A. C. Davies* 23
Fast context switches: compiler and architectural support for preemptive scheduling
*J. S. Snyder, D. B. Whalley and T. P. Baker* 35
Modelling the complexity of parallel and VLSI computations with Boolean circuits
*C. V. Papadopoulos and T. S. Andronikos* 43
A technique for process pre-emption in the transputer
*M. H. Cheung, K. M. Shea and F. C. M. Lau* 51
A static fault detection system for digital integrated circuits
*R. Nagarajan, Tan Le Lay and Goh Mei Lin* 57

**Number 2**

*Papers taken from ERA Report 93-0890*

Differences between civil and military electronic flight control systems
*G. Belcher* 67
A family of fault-tolerant systems: electrical flight controls, from Airbus A320/330/340 to future military transport aircraft
*D. Brière, C. Favre and P. Traverse* 75
Real-time Ada applications with silicon executives
*D. Brière and C. Bouvier* 83
EFA modular computer concept
*W. Straube* 89
Performance engineering – how well does it really work?
*K. P. Dawson and A. J. Lee* 95
A dual viewpoint software test tool
*M. A. Hennell and J. A. Prudom* 101

**Number 3**

High speed RS-232 fibre optic communication system for underwater remotely operated vehicles
*J. N. Lygouras, A. Kapsopoulos and Ph. G. Tsalides* 115
Performance analysis of disk cache write policies
*D. G. Miller and D. T. Harper III* 121
SHARP: a shape recognition system and its parallel implementation
*C. P. Ravikumar and R. Sethi* 131
VLSI design and implementation of systolic tree queues
*S. M. Sait and M. A. A. Khalid* 139
Advanced educational parallel DSP system based on TMS320C25 processors
*F. Kurugöllü, H. Palaz, H. Gümüskaya, E. Harmanci and B. Orencik* 147
A dynamically reconfigurable parallel processing system
*P. Lidstone, M. Horwood and J. Baker* 157
Cascade signature and syndrome compression
*R. E. Ahmed* 161

**Number 4**

Transputer implementation of interpolators for radar image transformations
*J. E. L. Hollis and T. E. Cronk* 179
A bit-level systolic implementation of the median filter
*Z. Hu and G. A. King* 185
Performance issues of a superscalar microprocessor
*S. Wallace and N. Bagherzadeh* 187
A self-selection distributed arbiter for a multiprocessor
*E. F. V. Martins and A. N. da Cruz* 201
A comprehensive study of digital signal processing devices
*R. Deka* 209
A RISC based protocol converter for IBM mainframes
*M. B. Akhan and O. A. Yedekcioglu* 223
A multilayered feed forward neural network suitable for VLSI implementation
*H. S. Mazumdar* 231

**Number 5**

Verification of hardware combining multiplication, division and square root
*C. D. Walter* 243
Design and VLSI implementation of an ASIC for real-time manipulation of digital colour images
*I. Andreadis, K. Stavroglu and Ph. Tsalides* 247
Design and implementation of an FPGA transponder
*B. H. Tan, E. Tan, K. T. Lau and S. C. Mar* 255
Holistic computing
*S. R. Wiseman and H. S. Field-Richards* 261
BEE: a special-purpose machine for hardware description language
*W. L. Loh* 269


0141-9331/95/$9.50 © 1995 Elsevier Science B.V. All rights reserved

Adaptive cosine transform coding for compression of Mars-96 ELISMA instrument
*W.-W. Lu and M. P. Gough* 277
Parallel implementations of convolution and moments algorithms on a multi-transputer system
*C. J. Turner, V. C. Bhavsar and P. R. Pochec* 283
CISC, RISC and DSP processors in real-time signal processing and control
*M. O. Tokhi and M. A. Hossain* 291

**Number 6**

SHEMUS: synthesis of heterogeneous multiprocessor systems
*M. K. Dhodhi, I. Ahmad and R. Storer* 311
A linear rotation based solution of large systems on a transputer array
*M. Chirico, E. Di Zitti and G. M. Bisio* 321
ASIC design of a matching unit for NLP
*S. Raman and E. R. Shaji* 327
Statistical analysis of parallel randomized algorithms for VLSI placement and implementation on workstation networks
*K. Efe* 341
Development of a real-time, 20 mega-samples per second, 32 channel data acquisition system
*A. M. MacLeod, P. F. Marin and W. A. Gillespie* 351
Design and implementation of a massively parallel architecture for high-level electronic measurements
*A. Gandelli and V. Piuri* 361

**Number 7**

Design and implementation of a scalable low-cost shared-memory multiprocessor system using IBM compatible PCs
*V. Lakshmi Narasimhan and S. Price-White* 383
A transputer based vehicle simulator
*T. Srikanthan, K. Y. Chan, H. S. Seah and S. K. Leong* 395
Parallelization of the stack
*P. A. Shallow* 405
Implementing distributed process farms
*A. Bartoli and G. Dini* 413
Optical character recognition using fuzzy logic
*W. A. Gowan* 423
Critical path analysis for field-programmable gate arrays 435

**Number 8**

TUTNC: a general purpose parallel computer for neural network computations
*T. Hämäläinen, J. Saarinen and K. Kaski* 447
An evolutionary technique for local microcode compaction
*I. Ahmad, M. K. Dhodhi and K. A. Saleh* 467
Fault tolerant process tracking in Lego
*L. Hughes and G. Stoddart* 475
Performance benefits and power/energy savings of 28F016XS-based system designs
*B. Dipert and K. McKee* 481
Power supplies for the Pentium, PowerPC and beyond 489

**Number 9**

*Special Section: Technical Applications Papers on Avionics Systems – Part One*

System development – the challenges of re-useability
*J. M. Kirby* 503
Method and specification tools for Airbus onboard systems
*D. Brière, D. Ribot, D. Pilaud and J.-L. Camus* 511
High integrity software development: process and tool issues
*A. D. Hutcheon, D. T. Jordan, J. A. McDermid, R. H. Pierce, I. C. Wand and B. J. Jepson* 517

Flexible kinematics for modular robots
*K. N. Tarchanidis, A. S. Mackay and J. Lucas* 525
FPGAs for expression level parallel processing
*R. Halverson, Jr and A. Lew* 533
Interfacing Inmos links to the ISA bus
*D. N. J. White* 541

**Number 10**

*Special Section: Technical Applications Papers on Avionics Systems – Part Two*

A comparison of standards for software engineering based on DO-178B for certification of avionics systems
*H. H. Hesselink* 559
Data flow oriented control law design with the graphical language HOSTESS
*A. Kröger* 565
ARINC 653 – Challenges of the present and future
*A. Cook* 575

DSP-based control of brushless DC drives for direct-driven robotic arms
*K. J. Tseng* 581
Heuristic fault-tolerant routing strategies for a multiprocessor network
*P. K. K. Loh* 591
Implementation of a RISC microprocessor for programmable logic controllers
*G. S. Roh, K. Koo, N. Chang, J. Park, Y. Kim and W. H. Kwon* 599
Improved RMS for the PC environment
*S. Savić, M. Tomašević, V. Milutinović, A. Gupta, M. Natale and I. Gertner* 609

## Author index

Ahmad, I. 311, 467
Ahmed, R. E. 161
Akhan, M. B. 223
Andreeadis, I. 247

Bagherzadeh, N. 187
Baker, J. 157
Bartoli, A. 413
Bauer, B. 83
Belcher, G. 67
Bhavsar, V. C. 283
Bisio, G. M. 321
Bouvier, C. 83
Brière, D. 75, 511

Camus, J.-L. 511
Chan, K. Y. 395
Chang, N. 599
Chirico, M. 321
Cook, A. 575
Cronk, T. E. 179

da Cruz, A. N. 201
Dawson, K. P. 95
Deka, R. 209
Dhodhi, M. K. 311, 467
Di Zitti, E. 321
Dini, G. 413
Dipert, B. 481

Efe, K. 341

Favre, C. 75
Field-Richards H. S. 261

Gandelli, A. 361
Gertner, I. 609
Gillespie, W. A. 351
Gough, M. P. 277
Gowan, W. A. 423
Gümüskaya, H. 147
Gupta, A. 609

Halverson Jr, R. 533
Hämäläinen, T. 447
Harmanci, E. 147
Harper III, D. T. 121
Hennell, M. A. 101
Hesselink, H. H. 559
Hollis, J. E. L. 179
Horwood, M. 157
Hossain, M. A. 291
Hu, Z. 185
Hughes, L. 475
Hutcheon, A. D. 517

Jepson, B. J. 517
Jordan, D. T. 517

Kapsopoulos, A. 115
Kaski, K. 447
Khalid, M. A. 139
Kim, Y. 599
King, G. A. 185
Kirby, J. M. 503
Koo, K. 599
Kröger, A. 565
Kurugöllü, F. 147
Kwon, W. H. 599

Lakshmi Narasimhan, V. 383
Lau, K. T. 255
Lee, A. J. 95
Leong, S. K. 395
Lew, A. 533
Lidstone, P. 157
Loh, P. K. 591
Loh, W. L. 269
Lu, W.-W. 277
Lucas, J. 525
Lygouras, J. N. 115

Mackay, A. S. 525
MacLeod, A. M. 351
Mar, S. C. 255
Marin, P. F. 351
Martins, E. F. V. 201
Mazumdar, H. S. 231
McDermid, J. A. 517
McKee, K. 481
Miller, D. G. 121
Milutinović, V. 609

Natale, M. 609

Orencik, B. 147

Palaz, H. 147
Park, J. 599
Pierce, R. H. 517
Pilaud, D. 511
Piuri, V. 361
Pochec, P. R. 283
Price-White, S. 383
Prudom, J. A. 101

Raman, S. 327
Ravikumar, C. P. 131
Rho, G. S. 599
Ribot, D. 511

Saarinen, J. 447
Sait, S. M. 139
Saleh, K. A. 467
Savić, S. 609
Seah, H. S. 395
Sethi, R. 131
Shaji, E. R. 327
Shallow, P. A. 405
Srikanthan, T. 395
Stavroglu, K. 247
Stoddart, G. 475
Storer, R. 311
Straube, W. 89

Tan, B. H. 255
Tan, E. 255
Tarchanidis, K. N. 525
Tokhi, M. O. 291
Tomašević, M. 609
Traverse, P. 75
Tsalides, Ph. 247
Tsalides, Ph. G. 115
Tseng, K. J. 581
Turner, C. J. 283

Wallace, S. 187
Walter, C. D. 243
Wand, I. C. 517
White, D. N. J. 541
Wiseman, S. R. 261

Yedekcioglu, O. A. 223

## Keyword index

**ARINC 653**
Integrated modular avionics 575
**ASIC**
Controller, Proportional plus integral 15
**ATN parser**
Lexicon, Natural language processing 327
**Automated layout**
VLSI design, Systolic tree architecture 139
**Avionics software systems**
Software development 559

**Battery management**
NiMH, NiCd 165
**Bit-level systolic array**
Digital signal processing, Median filter 185
**Board-level testing**
Syndrome analysing, Signature analyser 161
**Boolean circuits**
Lower bounds, Sequential complexity 43

**Coding**
Data compression, Telecommunications 277
**Colour**
Real-time, Image processing 247
**Complex instruction set computer**
Reduced instruction set computer, Digital signal processing 291
**Computer architecture**
Performance evaluation, RISC 187
**Computer arithmetic**
Redundant number systems, Recurrence relations 243
**Computer assisted specification**
Systems development 511
**Contention**
Multiprocessor, Self-selection arbiter 210
**Context switches**
Preempive scheduling, Register remapping 35
**Control engineering**
Robotics, Digital signal processor 581
**Controller**
Proportional plus integral, ASIC 15
**Critical path analysis**
Field programmable gate arrays, Timing constraints 435

**Data compression**
Telecommunications, Coding 277
**Data Interaction Architecture (DIA)**
MASCOT, Robotics 23
**Database**
Digital ICs, Fault detection 57
**Density estimation**
Randomized algorithms, Simulated annealing 341
**Digital ICs**
Fault detection, Database 57
**Digital signal processing**
Complex instruction set computer, Reduced instruction set computer 291
Median filter, Bit-level systolic array 185
Parallel processing, Parallel debugging 147
Control engineering, Robotics 581
**Disk caches**
Disk controllers, I/O traces 121
**Disk controllers**
I/O traces, Disk caches 121
**Distributed programming support**
Process farms, Message passing 413
**Distributed shared memory**
HDL-based simulation 609
**DSP benchmark**
DSP micro, DSP configuration 209
**DSP configuration**
DSP benchmark, DSP micro 209
**DSP micro**
DSP configuration, DSP benchmark 209

**Emulation**
RISC, Protocol conversion 223
**Evolutionary technique**
Microcode compaction, List scheduling 467

**Fast data capture**
Multiprocessor systems, OS-9 operating system 351
**Fault detection**
Database, Digital ICs 57
**Fault tolerance**
Parallel processing, Multiprocessors 591
Process tracking, Process migration 475
**Field programmable gate array (FPGA)**
Interrogation pulse, Transponder 255
Parallel processing, Image processing 533
Timing constraints, Critical path analysis 435
**Flash memory**
System performance, Power consumption 481
**Flexible control**
Inverse kinematics, Modular robots 525
**Fuzzy logic**
MC68HC11E9, Optical character recognition 423

**Genetic algorithms**
Minimum path configurations, Parallel processing 9

**Hardware description languages**
Reduced instruction set computers, Processor architecture 269
**HDL-based simulation**
Distributed shared memory 609
**High integrity software development**
Tool support, Software development 517
**High-level electronic measurements**
Multiprocessor design, Multiprocessor dedicated architecture 361

**Hough transform**
Shape recognition, Parallel algorithm 131

**I/O traces**
Disk caches, Disk controllers 121
**IBM PCs**
Shared memory, Synchronization 383
**Image processing**
Colour, Real-time 247
Field programmable gate arrays, Parallel processing 533
Parallel processing, Transputers 283
**Inmos links**
Transputers, ISA bus 541
**Integrated modular avionics**
ARINC 653 575
**Interconnection network**
Parallel processing, Reconfiguration 157
**Interfacing**
Real-time, Transputers 3
**Interrogation pulse**
Transponder, Field programmable gate array (FPGA) 255
**Inverse kinematics**
Modular robots, Flexible control 525
**ISA bus**
Inmos links, Transputers 541

**Large systems**
Linear rotation, Transputer arrays 321
**Lexicon**
Natural language processing, ATN parser 327
**Linear rotation**
Transputer arrays, Large systems 321
**List scheduling**
Evolutionary technique, Microcode compaction 467
**Load balancing**
Rendering, Vehicle simulator 395
**Lower bounds**
Sequential complexity, Boolean circuits 43

**MASCOT**
Robotics, Data Interaction Architecture (DIA) 23
**MC68HC11E9**
Optical character recognition, Fuzzy logic 423
**Median filter**
Bit-level systolic array, Digital signal processing 185
**Message passing**
Distributed programming support, Process farms 413
**Microcode compaction**
List scheduling, Evolutionary technique 467
**Microprocessors**
Voltage levels, Power supplies 489
**Minimum path configurations**
Parallel processing, Genetic algorithms 9
**Modular robots**
Flexible control, Inverse kinematics 525
**Multi-processor image rotation**
Synthetic aperture radar image processing, Transputer optimization 179
**Multilayer neural network**
VLSI, Stochastic 231
**Multiprocessor**
Self-selection arbiter, Contention 210
**Multiprocessor dedicated architecture**
High-level electronic measurements, Multiprocessor design 361
**Multiprocessor design**
Multiprocessor dedicated architecture, High-level electronic measurements 361
**Multiprocessor systems**
OS-9 operating system, Fast data capture 351
**Multiprocessors**
Fault tolerance, Parallel processing 591
Synthesis, Scheduling and allocation 311

**Natural language processing**
ATN parser, Lexicon 327
**Neural networks**
Tree shape architecture, Parallel computing 447
**NiCd**
Battery management, NiMH 165
**NiMH**
NiCd, Battery management 165

**Operating system**
Process pre-emption, Real-time computing 51
**Optical character recognition**
Fuzzy logic, MC68HC11E9 423
**OS-9 operating system**
Fast data capture, Multiprocessor systems 351

**Parallel algorithm**
Hough transform, Shape recognition 131
**Parallel computing**
Neural networks, Tree shape architecture 447
**Parallel debugging**
Digital signal processing, Parallel processing 147
**Parallel processing**
Genetic algorithms, Minimum path configurations 9
Image processing, Field programmable gate arrays 533
Multiprocessors, Fault tolerance 591
Parallel debugging, Digital signal processing 147
Reconfiguration, Interconnection network 157
Transputers, Image processing 283
**Performance evaluation**
RISC, Computer architecture 187
**Position control**
RS-232 communication protocol, Remotely operated vehicle 115
**Power consumption**
Flash memory, System performance 481
**Power supplies**
Microprocessors, Voltage levels 489
**Preemptive scheduling**
Register remapping, Context switches 35
**Process farms**
Message passing, Distributed programming support 413
**Process migration**
Fault-tolerance, Process tracking 475
**Process pre-emption**
Real-time computing, Operating system 51
**Process tracking**
Process migration, Fault-tolerance 475
**Processor architecture**
Hardware description languages, Reduced instruction set computers 269
**Programmable logic controllers**
RISC architecture, Special purpose microprocessor 599
**Proportional plus integral**
ASIC, Controller 15
**Protocol conversion**
Emulation, RISC 223

**Randomized algorithms**
Simulated annealing, Density estimation 341
**Re-useability**
System development 503
**Real-time**
Image processing, Colour 247
Transputers, Interfacing 3
**Real-time computing**
Operating system, Process pre-emption 51
**Reconfiguration**
Interconnection network, Parallel processing 157
**Recurrence relations**
Computer arithmetic, Redundant number systems 243
**Recursion**
Stack allocation, Threads 405
**Reduced instruction set computer**
Digital signal processing, Complex instruction set computer 291
Processor architecture, Hardware description languages 269
**Redundant number systems**
Recurrence relations, Computer arithmetic 243
**Register remapping**
Context switches, Preemptive scheduling 35
**Remotely operated vehicle**
Position control, RS-232 communication protocol 115
**Rendering**
Vehicle simulator, Load balancing 395

**RISC**
Computer architecture, Performance evaluation 187
Protocol conversion, Emulation 223
Stack architecture, Stack cache 261
**RISC architecture**
Special purpose microprocessor, Programmable logic controllers 599
**Robotics**
Data Interaction Architecture (DIA), MASCOT 23
Digital signal processor, Control engineering 581
**RS-232 communication protocol**
Remotely operated vehicle, Position control 115

**Scheduling and allocation**
Multiprocessors, Synthesis 311
**Self-selection arbiter**
Contention, Multiprocessor 210
**Sequential complexity**
Boolean circuits, Lower bounds 43
**Shape recognition**
Parallel algorithm, Hough transform 131
**Shared memory**
Synchronization, IBM PCs 383
**Signature analyser**
Board-level testing, Syndrome analysing 161
**Simulated annealing**
Density estimation, Randomized algorithms 341
**Software development**
High integrity software development, Tool support 517
Avionics software systems 559
**Special purpose microprocessor**
Programmable logic controllers, RISC architecture 599
**Stack allocation**
Threads, Recursion 405
**Stack architecture**
Stack cache, RISC 261
**Stack cache**
RISC, Stack architecture 261
**Stochastic**
Multilayer neural network, VLSI 231
**Synchronization**
IBM PCs, Shared memory 383
**Syndrome analysing**
Signature analyser, Board-level testing 161
**Synthesis**
Scheduling and allocation, Multiprocessors 311
**Synthetic aperture radar image processing**
Transputer optimization, Multi-processor image rotation 179
**System development**
Re-useability 503
**System performance**
Power consumption, Flash memory 481
**Systems development**
Computer assisted specification 511
**Systolic tree architecture**
Automated layout, VLSI design 139

**Telecommunications**
Coding, Data compression 277
**Threads**
Recursion, Stack allocation 405
**Timing constraints**
Critical path analysis, Field programmable gate arrays 435
**Tool support**
Software development, High integrity software development 517
**Transponder**
Field programmable gate array (FPGA), Interrogation pulse 255
**Transputer optimization**
Multi-processor image rotation, Synthetic aperture radar image processing 179
**Transputers**
Image processing, Parallel processing 283
Interfacing, Real-time 3
ISA bus, Inmos links 541
**Tree shape architecture**
Parallel computing, Neural networks 447

**Vehicle simulator**
Load balancing, Rendering 395
**VLSI**
Stochastic, Multilayer neural network 231
**VLSI design**
Systolic tree architecture, Automated layout 139
**Voltage levels**
Power supplies, Microprocessors 489

**Book review** 105

**Letter to the editor** 235